

Fig. 1

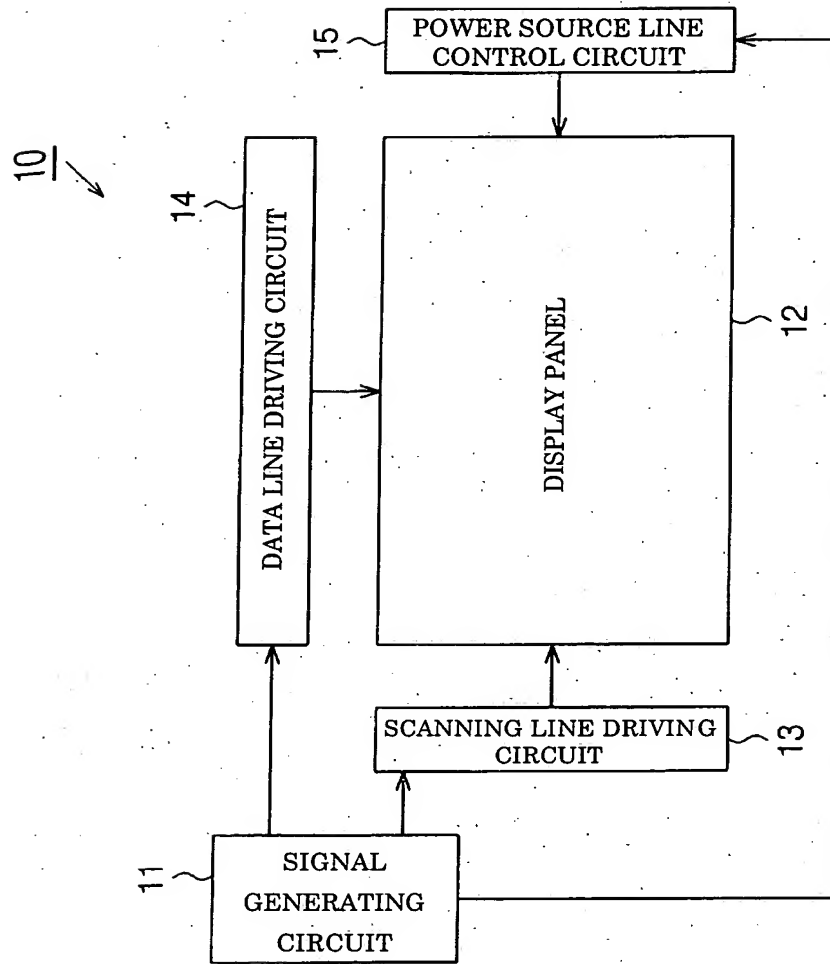


Fig. 2

The diagram illustrates a display device circuit. At the top, a horizontal block labeled 'POWER SOURCE LINE CONTROL CIRCUIT' is connected to a series of vertical lines labeled SC1, SC2, ..., SCn. At the bottom, a horizontal block labeled 'SCANNING LINE DRIVING CIRCUIT' is connected to a series of horizontal lines labeled SY1, SY2, ..., SYN. The intersection of these lines forms a grid of pixels. Each pixel is represented by a rectangular block containing a diode symbol (triangle pointing towards the top-right) and two terminals labeled 20 and 21. The horizontal lines are also labeled X1, X2, X3, ..., XM, and the vertical lines are labeled Y1, Y2, ..., YN. Data lines are shown as horizontal lines labeled Idata1, Idata2, Idata3, ..., IdataM, with arrows indicating the direction of data flow. The circuit is further divided into sections by dashed lines, with labels like Vd, Vb, and Vc indicating different voltage levels or control signals. The overall layout is a rectangular grid with additional control and data lines extending from the top and bottom blocks.

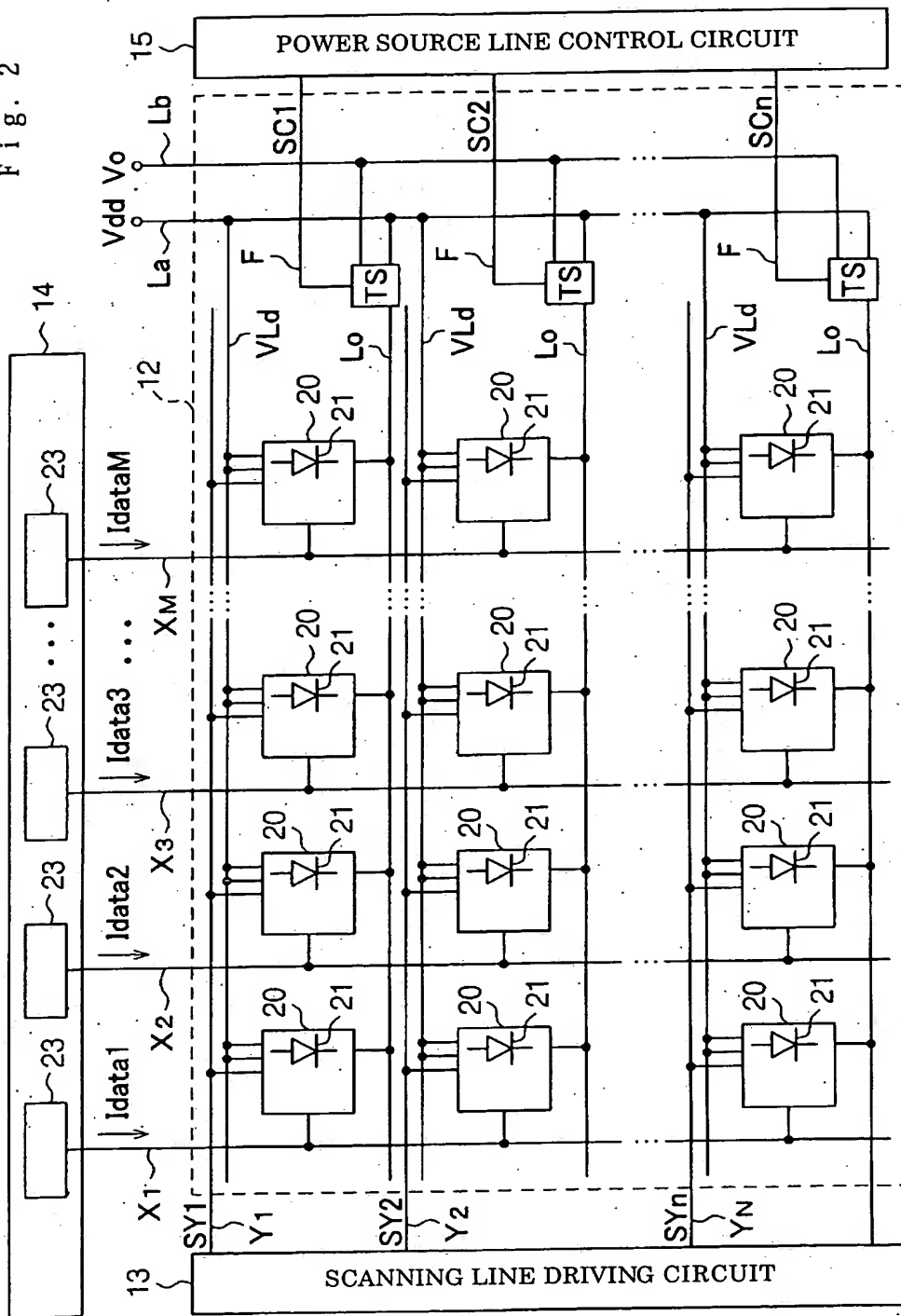


Fig. 5

The diagram illustrates a display device architecture. At the bottom, a **SCANNING LINE DRIVING CIRCUIT** (13) provides scanning signals $Y_1, Y_2, Y_3, \dots, Y_N$ to a grid of pixels. On the left, a **DATA LINE DRIVING CIRCUIT** (14) provides data signals X_1, X_2, \dots, X_M to the same grid. Each pixel is formed by a combination of a data transistor (20R, 20G, or 20B) and a scanning transistor (20R, 20G, or 20B), connected to a common data line (Lo) and a common scanning line (Vld). A power source line control circuit (15) at the top manages the power supply lines $V_{ddB}, V_{ddG}, V_{ddR}$ and the output line V_o . The circuit includes various components such as transistors (TS), capacitors (C), and resistors (R). Labels LaB, LaG, LaR, Lb indicate specific regions or components within the display area.

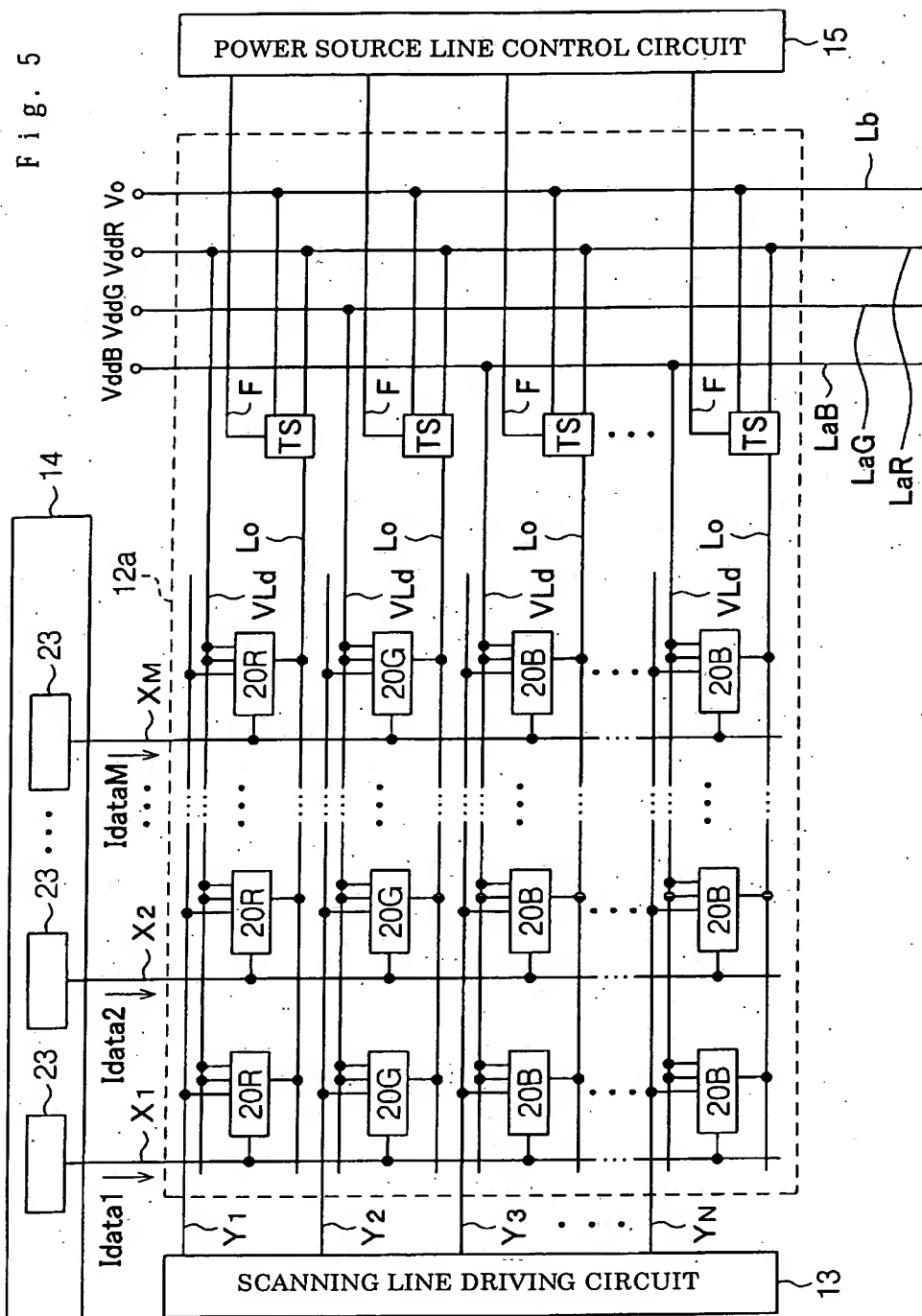


Fig. 6

